**A GENERAL PURPOSE REAL-TIME SoC BASED MATRIX CALCULATOR**

**Project**

**ECE 5730 –Embedded System Design Using FPGAs**

**Submitted by**

**Cory Ness**

**Kokila Subramanian**

**Shivani Devatha**

**Submitted to**

**Professor Subramaniam Ganesan**



**Fall 2021**

**Table of Contents**

[Abstract 3](#_Toc89686015)

[Objective 4](#_Toc89686016)

[System-level Block Diagram 4](#_Toc89686017)

[Hardware Components 4](#_Toc89686018)

[**UART-TTL Converter:** 5](#_Toc89686019)

[**DE1-SoC FPGA Development Kit:** 5](#_Toc89686020)

[Matrix Manipulation Theory 6](#_Toc89686021)

[**Pseudo code for Matrix Addition:** 6](#_Toc89686022)

[**Pseudo code for Matrix Subtraction** 6](#_Toc89686023)

[**Pseudo code for Multiplication:** 7](#_Toc89686024)

[**Pseudo code for Transpose of Matrix:** 8](#_Toc89686025)

[**Pseudo code for Determinant of Matrix:** 8](#_Toc89686026)

[Algorithm 10](#_Toc89686027)

[**Algorithm for UART Decoder:** 10](#_Toc89686028)

[**Algorithm for UART Transmitter:** 10](#_Toc89686029)

[**Algorithm for FIFO:** 11](#_Toc89686030)

[**Algorithm for Matrix Calculator:** 12](#_Toc89686031)

[Results 13](#_Toc89686032)

[Conclusion 14](#_Toc89686033)

[Future improvements 14](#_Toc89686034)

[References 15](#_Toc89686035)

[Appendix 16](#_Toc89686036)

[**Code** 16](#_Toc89686037)

[**VHDL code for TOP level entity** 16](#_Toc89686038)

[**VHDL code for MATRIX\_CALCULATOR\_sys** 17](#_Toc89686039)

[**VHDL code for UART Decoder** 44](#_Toc89686040)

[**VHDL code for UART Transmitter:** 45](#_Toc89686041)

[**VHDL code for FIFO:** 47](#_Toc89686042)

[**Nios C code:** 49](#_Toc89686043)

Abstract

Matrix manipulation includes operations such as addition, subtraction, multiplication, inverse, and transpose etc., on the array of data stored as rows and columns. It is an essential process used in diverse fields of science and commerce including but not limited to Computer technology, Optics, Geology, Cryptography, Network Theory, Robotics and Animations, and Finance. Real-time matrix operations include a large number of computations, required for process control, and data & signal processing, which directly impacts the system performance. Real-time matrix calculation becomes a bottleneck for performance of fast system applications as it requires large computation power, memory, and time.

In this project, we present a design which can perform matrix manipulations such as addition, subtraction, scalar and matrix array multiplication, determinant of matrix, co-factor and other vital matrix operations required for real-time signal processing. The matrix manipulator is developed using Intel DE1-SoC development board with Cyclone V processor is interfaced with FT232R FTDI UART to establish serial communication between the FPGA board and PC. The matrix calculator is implemented in the NIOS II soft-core processor present on DE1-SoC board, the inputs are fed from a host computer onto FPGA board via UART serial port, a USB to TTL convertor module will be used to establish serial communication. The final computational results are fetched using the serial communication onto the remote PC.

Objective

Real-time signal processing system involves large computations and complex process control operations on massive array of data which is highly time-consuming. Currently, most of matrix operations are performed using software. The expansion of matrix dimension and reduction in processing speed has become bottleneck for the most of the existing real-time fast system applications. The objective of this project is to develop a Real-time Matrix-Manipulator using UART to TTL convertor for serial communication, Intel DE1-SoC FPGA Development Kit, and TRDB- TLM Touch screen LCD Display. The input matrix values are served into the FPGA board using Serial communication from a remote system. The matrix operations are executed in NIOS-II processor available in DE1-SoC board. The manipulated resultant matrix is displayed in the LCD display. The NIOS –II processor is used to control system operation and perform basic matrix operations such as addition, subtraction, Multiplication, finding determinant, co-factor, and other essential matrix operations required for real-time signal processing.

System-level Block Diagram

The system-level Block diagram for the Real-time Matrix Manipulator is shown in figure 1. The major functional blocks include the Remote PC, UART TTL convertor, the DE1-SoC board and the TRDB-TLM LCD display.



SDRAM

UART RX

NIOS II

Matrix Operation Algorithm

SSRAM

UART TX

UART

PIO

**USB to UART**

Serial communication

**DE1-SoC**

**PC**

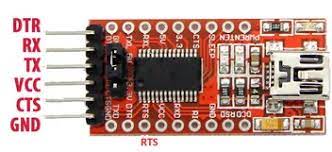
**Figure 1: System-level Block Diagram**

Hardware Components

The developed Real-Time Matrix Manipulator consists of the following hardware components:

1. UART-TTL Convertor – FT232R FTDI
2. DE1-SoC Development Kit

**UART-TTL Converter:**

******

**Figure 2. FT232R FTDI USB UART**

The USB UART-TTL converter used is an FT232R FTDI (Future Technology Device International Ltd.) chip on a breakout board that simplifies serial communication by reducing the external components. Figure 2 shows the package of the USB UART. It is a fully integrated chip with 1024-bit EEPROM, clock generation, and USB termination resistors. The FT232R serial UART can support data rate transfer rates from 300 baud to 3 Mbaud at the TTL levels (FT232R, n.d.). High data throughput is achieved through the 128 bytes receive buffer and the 256 bytes transmit buffer that utilizes smooth buffer technology. The UART interface will support 7 or 8 data bits with 1 or 2 bits for representing odd, even, mark, space and non-parity bits (FT232R, n.d.). The configurable I/O pins integrated +3.3V level convertor provides output drive strength for various applications. It can be used as interface with MCU/ PLD/FPGA based designs, PDA to USB data transfer, smart card readers, Industrial control, Hardware and Wireless modems, Bar Code Readers, and Cellular Phone USB data transfer cables and interfaces ((FT232R, n.d.).

The communication is established by making use of the UART Rx and Tx lines going to pins 1 and 3 on the 20-pin expansion header of DE1-SoC board. It allows any computer to open a serial port and communicate to the DE1-SoC over a COM port, inputting the equations needed for the Matrix equations. In addition, the DE1-SoC can transmit data back to the computer by sending UART data to the FTDI board, which will display on the serial port screen for the user.

**DE1-SoC FPGA Development Kit:**

The DE1-Soc Development kit provides a hardware platform that combines the System-on Chip (SoC) FPGA and dual-core Cyclone- A9 embedded core which can be used for wide industrial application improvement. It provides users the power of flexibility in design, paired with high-processor, low-power processing system. It provides seamless integration of both SoC and ARM based hard processor system (HPS), including processor, memory and peripheral interfaces over a high-bandwidth interconnect backbone. The DE1SoC board includes hardware such as high-speed DDR3 memory, video and audio capability, Ethernet, networking and much more.

Matrix Manipulation Theory

Matrices are representation of array of data commonly used in extensive real-world data processing, research, and scientific studies. Matrix Multiplication provides good approximation for complicated calculation of real-time sensitive engineering applications signal processing, image processing, network theory and many more. Matrix manipulation is engaged with every part of day-to-day life including data base management, encryption that helps security, 3D gaming, robotics and animation, create models for economic and business, construction, physics, and geology. The common matric calculations involved are addition, subtraction, multiplication, transpose, finding the determinant value and inverse of the matrix.

**Pseudo code for Matrix Addition:**

Matrix addition can be performed only when both the matrices under operation are of same size. It is commonly employed in data, image and signal processing. The void matrix\_addition() performs the following activity:

for (i=0;i<r1;i++)

{

for (j=0;j<c1;j++)

{

res[i][j]= a[i][j]+b[i][j];

}

}

**Pseudo code for Matrix Subtraction**

Matrix subtraction is a linear algebraic operation which can be performed only when both the matrices under operation are of same size. The void matrix\_subraction() performs the following operation:

for (i=0;i<r1;i++)

{

for (j=0;j<c1;j++)

{

res[i][j]= a[i][j]-b[i][j];

}

}

**Pseudo code for Multiplication:**

Matrix Multiplication can be either scalar or matrix multiplication, and is the most challenging algebraic operation. Matrix multiplication can be either scalar, vector or matrix multiplication. Scalar multiplication is a element-wise multiplication of matrix elements using a real or complex value. In the below defined code, *void scalar\_matrix\_multiplication()* executes matrix multiplication using constant value k.

for (i=0;i<r1;i++)

{

for (j=0;j<c1;j++)

{

res[i][j] = k\*a[i][j];

}

}

Multiplication of matrices can be executed under the condition that the number of rows of first matrix should be equal to number of columns in the second matrix (i.e. [A]i x j\* [B]m x n = [C]i x n.

if (r1 != c2)

{

printf("Matrix multiplication cannot be performed\n");

}

else

for (i=0;i<r1;i++)

{

for (j=0;j<c2;j++)

{

res[i][j]=0;

for (k=0; k<c1;k++)

res[i][j] += a[i][k]\*b[k][j];

}

}

**Pseudo code for Transpose of Matrix:**

Transpose is simply interchanging the rows and columns. It is generally employed when multiple matrix exists and the dimensions without transposing is not amendable for matrix operations. In real-time one usage of transpose is data manipulation, where the application requires the use of orthonormal matrix. In image processing switching rows and columns of pixels can result in exchanging the domain and space of the image transformation. In neural networks, frequent process weight and inputs of different sizes where the dimensions do not meet the requirement of algorithm can be accomplished using simple transpose of matrix.

for (i=0;i<c1;i++)

{

for (j=0;j<r1;j++)

{

res[i][j] = a[j][i];

}

}

**Pseudo code for Determinant of Matrix:**

Determinant is the number associated with square matrix that encodes information about the matrix. Determinant of matrix is used to check the consistency of any system and to solve linear equations.

for (int f = 0; f < n; f++)

{

// Getting Cofactor of a[0][f]

temp= malloc(2\*sizeof\*temp);

for (i=0; i< 2; i++)

{

temp[i]= malloc(2\*sizeof\*temp[i]);

}

i=0;

// Looping for each element of the matrix

for (int row = 0; row < n; row++)

{

for (int col = 0; col < n; col++)

{

// Copying into temporary matrix only those

// element which are not in given row and

// column

if (row != 0 && col != f)

{

temp[i][j++] = a[row][col];

// Row is filled, so increase row index and

// reset col index

if (j == n - 1)

{

j = 0;

i++;

}

}

}

}

if(f%2==0)

{

(D += a[0][f]\*(matrix\_det(temp, n - 1,n - 1)));

}

else

{

D -= a[0][f]\*(matrix\_det(temp, n - 1,n - 1));

}

// terms are to be added with alternate sign

D1=D;

Algorithm

**Algorithm for UART Decoder:**

The UART Decoder accepts 2 inputs and has 2 outputs. The first input is Clk, with a frequency set by the generic variable ClockRate. The second input is Rx, which is the pin state of the UART Rx pin. The first output is Complete, a single bit that is low while receiving Uart data and high once the Uart byte is fully decoded. The second output is Data, an 8-bit vector that is decoded value from the Rx pin. The VHDL code for the UART decoder works as follows:

1. Input the clock rate and baud rate using the generic map, as this will not change throughout operation.
2. Wait for the start-bit from UART Rx (High->Low Transition).
3. Begin counting the clock cycles until we reach the necessary baud rate.
4. Halfway-through the count, sample the Rx line and save it in data\_register, this ensures we sample when the data line is stable.
5. Once the count reaches the baud value, reset the count
6. Repeat until all 10 bits have been sampled (start bit, data bits, stop bit).
7. Once all bits have been sampled, set the Complete signal to indicate Data is stable
8. Wait for next start-bit.

This isn’t sufficient, however, for the NIOS processor to use, since it will stream all the data in immediately. We can make use of interrupts inside the NIOS processor to react whenever the Complete signal rises, but it will take time away from performing calculations. We decided to make use of the decoder by also implementing a FIFO (First In First Out) buffer, which will buffer in up to 128 bytes of UART data to be read out by the NIOS processor when it’s ready.

**Algorithm for UART Transmitter:**

The VHDL code for the UART transmitter is very similar to the Decoder, but in reverse. It has 3 inputs and a single output. The first input is Clk, the system clock with frequency specified in the generic ClockRate. The second input is Send, a single bit that triggers the send sequence on a low to high transition. The third input is Data, an 8-bit vector that is the value to send over UART. It also has a single output, Tx, which should be tied to the Tx pin on the DE1 board. The transmitter works as follows:

1. Input clock rate and baud rate using generic map, as this will not change throughout operation
2. Wait for low->high transition on Send input
3. Bring Tx low, and begin counting clock cycles until we reach necessary baud rate
4. Once the count has rolled over, change the Tx state based on the bit of Data
5. Repeat until all 8 data bits have been sent
6. Bring Tx high to send the stop bit.
7. Reset all variables back to original states and wait for next low->high transition.

Following this we can control the transmitter tying a parallel IO in the NIOS processor to send the start signal, and the data can be tied to another parallel IO. The Clk and Tx bits are tied to the 50 Mhz clock and UART Tx pin respectively, and this is everything necessary to integrate a UART transmitter into our NIOS design.

**Algorithm for FIFO:**

The VHDL code for the FIFO is very simple and elegant. It uses 4 inputs and 1 output. The first input is complete, which indicates that data is complete and ready to be pushed into the FIFO. The next is data\_in, an 8 bit vector that is the data to be pushed in. The third is pop, which will pop out the data and point data\_out to the next data to be sent out. The final input is clear, which clears and resets the FIFO so that it’s as if it had just started. The only output of the FIFO is data\_out, an 8-bit vector that is the data to be sent out. The operation for the FIFO is very simple, first configure the generic num to the amount of data you want to buffer. Then, tie the data\_in signal to some data you want buffered, and whenever you press complete, it will be buffered into the FIFO. Meanwhile, data\_out is always the oldest data in the buffer, and you can point data\_out to the next oldest data by pressing pop. Clear can be tied to a debug pin so that you can manually clear the FIFO during development. The process for the FIFO is as follows:

1. Configure the depth of the FIFO with the num generic value
2. Wait for low->high transition on the complete input or pop input or clear input
3. If low->high on complete…
   1. Copy data\_in into the mem (an array of size num of 8-bit vectors) signal at location start
   2. Increment start by one
4. If low->high on pop…
   1. Increment stop by one
5. If low->high on clear…
   1. Set start and stop both to 0
6. Check if start is equal to stop
7. If yes…
   1. Output “00000000”
8. Otherwise…
   1. Output the value in mem at location stop

**Algorithm for Matrix Calculator:**

The NIOS C code for calculator can read matrix of any order and can implement addition, subtraction, multiplication, transpose and also calculates determinant. Order of two matrices, values into two matrices and type of operation needs to be entered into a FIFO and when C code is built and run, the values are fetched into rows, columns and as elements of two matrices. The row and column sizes are dynamically allocated. So, there is no restriction on the order of the matrices. The process is as follows:

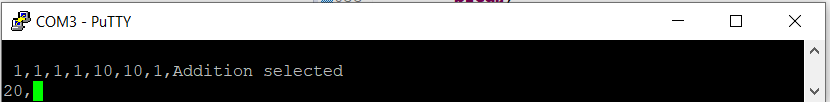
1. Inside main, declare variables that store row and column numbers of two matrices, chooses type of operation, array elements
2. Values into variables are read by decoding the values from parallel IO, which in turn fetches the value from FIFO
3. A function is used to indicate next value from parallel IO to be read
4. Based on the operation selected, the corresponding C function is called
5. Matrix operation is performed, and result is written into a parallel IO which is connected UART Tx and the results are displayed on the remote terminal

Results

Case 1: Two matrices of order (1,1)

A(1,1)=10; B(1,1)=10

Option selected: Addition

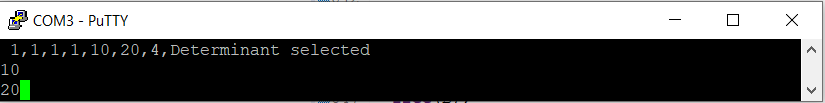


Output: Sum of 10+10 = 20

Case 2: Two matrices of order(1,1)

A(1,1)=10;B(1,1)=20;

Option selected: Determinant

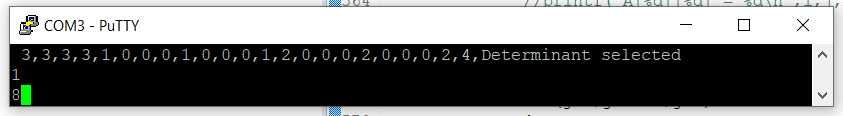


Output: Determinant of matrix A is 10; Determinant of matrix B is 20

Case 3: Two matrices of order(3,3)

A(3,3)=1,0,0;0,1,0;0,0,1;B(3,3)=2,0,0;0,2,0;0,0,2;

Option selected: Determinant



Output: Determinant of matrix A is 1; Determinant of matrix B is 8

Conclusion

Primary goal to use Nios II soft core processor and establish UART communication with USB to TTL converter interface is successfully achieved. There is no constraint on the amount of input data that can be read using UART within the hardware capability.

Future improvements

1. The matrix operations can be made generic to deal with different formats of data like float, double etc
2. The speed of UART Rx and Tx can be improved, the decoder can be made more robust to read large amount of data correctly
3. Extensive validation of the code was not feasible within the project timeline

References

1. *Future Technology Devices International LTD FT232R USB ...* (n.d.). <https://ftdichip.com/wp-content/uploads/2020/08/DS_FT232R.pdf>.
2. *DE1-SoC User Manual.*

[*https://www.intel.com/content/dam/altera-www/global/en\_US/portal/dsn/42/doc-us-dsnbk-42-1004282204-de1-soc-user-manual.pdf*](https://www.intel.com/content/dam/altera-www/global/en_US/portal/dsn/42/doc-us-dsnbk-42-1004282204-de1-soc-user-manual.pdf)

1. *Nios-II software development.*

[*https://www.uio.no/studier/emner/matnat/fys/FYS4220/h20/lecture-slides/embedded\_niosii\_sw\_dev.pdf*](https://www.uio.no/studier/emner/matnat/fys/FYS4220/h20/lecture-slides/embedded_niosii_sw_dev.pdf)

Appendix

**Code**

**VHDL code for TOP level entity**

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity MATRIX\_CALCULATOR is

port (

CLOCK\_50 : in std\_logic := '0'; -- clk.clk

UART\_RX : in std\_logic;

SW : in std\_logic\_vector(9 downto 0);

UART\_TX : out std\_logic;

LEDR : out std\_logic\_vector(9 downto 0)

);

end entity MATRIX\_CALCULATOR;

architecture Behavior of MATRIX\_CALCULATOR is

signal next\_write : std\_logic\_vector(7 downto 0);

signal toWrite : std\_logic\_vector(7 downto 0);

signal next\_read : std\_logic\_vector(7 downto 0);

signal toRead : std\_logic\_vector(7 downto 0);

signal gotUart : std\_logic;

signal decodedRead: std\_logic\_vector(7 downto 0);

component MATRIX\_CALCULATOR\_sys is

port (

clk\_clk : in std\_logic := '0'; -- clk.clk

nextval\_external\_connection\_export : out std\_logic\_vector(7 downto 0); -- nextval\_external\_connection.export

nextwriteval\_external\_connection\_export : out std\_logic\_vector(7 downto 0); -- nextwriteval\_external\_connection.export

readval\_external\_connection\_export : in std\_logic\_vector(7 downto 0) := (others => '0'); -- readval\_external\_connection.export

writeval\_external\_connection\_export : out std\_logic\_vector(7 downto 0) -- writeval\_external\_connection.export

);

end component;

begin

calculator : MATRIX\_CALCULATOR\_sys port map (CLOCK\_50, next\_read, next\_write, toRead, toWrite);

uart\_decoder : entity work.Uart\_Decoder port map (CLOCK\_50, UART\_RX, gotUart, decodedRead);

uart\_transmitter : entity work.Uart\_Transmitter port map (CLOCK\_50, next\_write(0), toWrite, UART\_TX);

read\_fifo : entity work.FIFO generic map (128) port map (gotUart, decodedRead, next\_read(0), SW(0), toRead);

LEDR(7 downto 0) <= toRead;

end Behavior;

**VHDL code for MATRIX\_CALCULATOR\_sys**

-- MATRIX\_CALCULATOR.vhd

-- Generated using ACDS version 18.1 625

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.numeric\_std.all;

entity MATRIX\_CALCULATOR\_sys is

port (

clk\_clk : in std\_logic := '0'; -- clk.clk

nextval\_external\_connection\_export : out std\_logic\_vector(7 downto 0); -- nextval\_external\_connection.export

nextwriteval\_external\_connection\_export : out std\_logic\_vector(7 downto 0); -- nextwriteval\_external\_connection.export

readval\_external\_connection\_export : in std\_logic\_vector(7 downto 0) := (others => '0'); -- readval\_external\_connection.export

writeval\_external\_connection\_export : out std\_logic\_vector(7 downto 0) -- writeval\_external\_connection.export

);

end entity MATRIX\_CALCULATOR\_sys;

architecture rtl of MATRIX\_CALCULATOR\_sys is

component MATRIX\_CALCULATOR\_jtag\_uart\_0 is

port (

clk : in std\_logic := 'X'; -- clk

rst\_n : in std\_logic := 'X'; -- reset\_n

av\_chipselect : in std\_logic := 'X'; -- chipselect

av\_address : in std\_logic := 'X'; -- address

av\_read\_n : in std\_logic := 'X'; -- read\_n

av\_readdata : out std\_logic\_vector(31 downto 0); -- readdata

av\_write\_n : in std\_logic := 'X'; -- write\_n

av\_writedata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- writedata

av\_waitrequest : out std\_logic; -- waitrequest

av\_irq : out std\_logic -- irq

);

end component MATRIX\_CALCULATOR\_jtag\_uart\_0;

component MATRIX\_CALCULATOR\_nextval is

port (

clk : in std\_logic := 'X'; -- clk

reset\_n : in std\_logic := 'X'; -- reset\_n

address : in std\_logic\_vector(1 downto 0) := (others => 'X'); -- address

write\_n : in std\_logic := 'X'; -- write\_n

writedata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- writedata

chipselect : in std\_logic := 'X'; -- chipselect

readdata : out std\_logic\_vector(31 downto 0); -- readdata

out\_port : out std\_logic\_vector(7 downto 0) -- export

);

end component MATRIX\_CALCULATOR\_nextval;

component MATRIX\_CALCULATOR\_nios2\_gen2\_0 is

port (

clk : in std\_logic := 'X'; -- clk

reset\_n : in std\_logic := 'X'; -- reset\_n

reset\_req : in std\_logic := 'X'; -- reset\_req

d\_address : out std\_logic\_vector(17 downto 0); -- address

d\_byteenable : out std\_logic\_vector(3 downto 0); -- byteenable

d\_read : out std\_logic; -- read

d\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

d\_waitrequest : in std\_logic := 'X'; -- waitrequest

d\_write : out std\_logic; -- write

d\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

debug\_mem\_slave\_debugaccess\_to\_roms : out std\_logic; -- debugaccess

i\_address : out std\_logic\_vector(17 downto 0); -- address

i\_read : out std\_logic; -- read

i\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

i\_waitrequest : in std\_logic := 'X'; -- waitrequest

irq : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- irq

debug\_reset\_request : out std\_logic; -- reset

debug\_mem\_slave\_address : in std\_logic\_vector(8 downto 0) := (others => 'X'); -- address

debug\_mem\_slave\_byteenable : in std\_logic\_vector(3 downto 0) := (others => 'X'); -- byteenable

debug\_mem\_slave\_debugaccess : in std\_logic := 'X'; -- debugaccess

debug\_mem\_slave\_read : in std\_logic := 'X'; -- read

debug\_mem\_slave\_readdata : out std\_logic\_vector(31 downto 0); -- readdata

debug\_mem\_slave\_waitrequest : out std\_logic; -- waitrequest

debug\_mem\_slave\_write : in std\_logic := 'X'; -- write

debug\_mem\_slave\_writedata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- writedata

dummy\_ci\_port : out std\_logic -- readra

);

end component MATRIX\_CALCULATOR\_nios2\_gen2\_0;

component MATRIX\_CALCULATOR\_onchip\_memory2\_0 is

port (

clk : in std\_logic := 'X'; -- clk

address : in std\_logic\_vector(13 downto 0) := (others => 'X'); -- address

clken : in std\_logic := 'X'; -- clken

chipselect : in std\_logic := 'X'; -- chipselect

write : in std\_logic := 'X'; -- write

readdata : out std\_logic\_vector(31 downto 0); -- readdata

writedata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- writedata

byteenable : in std\_logic\_vector(3 downto 0) := (others => 'X'); -- byteenable

reset : in std\_logic := 'X'; -- reset

reset\_req : in std\_logic := 'X'; -- reset\_req

freeze : in std\_logic := 'X' -- freeze

);

end component MATRIX\_CALCULATOR\_onchip\_memory2\_0;

component MATRIX\_CALCULATOR\_readval is

port (

clk : in std\_logic := 'X'; -- clk

reset\_n : in std\_logic := 'X'; -- reset\_n

address : in std\_logic\_vector(1 downto 0) := (others => 'X'); -- address

readdata : out std\_logic\_vector(31 downto 0); -- readdata

in\_port : in std\_logic\_vector(7 downto 0) := (others => 'X') -- export

);

end component MATRIX\_CALCULATOR\_readval;

component MATRIX\_CALCULATOR\_mm\_interconnect\_0 is

port (

clk\_0\_clk\_clk : in std\_logic := 'X'; -- clk

nios2\_gen2\_0\_reset\_reset\_bridge\_in\_reset\_reset : in std\_logic := 'X'; -- reset

nios2\_gen2\_0\_data\_master\_address : in std\_logic\_vector(17 downto 0) := (others => 'X'); -- address

nios2\_gen2\_0\_data\_master\_waitrequest : out std\_logic; -- waitrequest

nios2\_gen2\_0\_data\_master\_byteenable : in std\_logic\_vector(3 downto 0) := (others => 'X'); -- byteenable

nios2\_gen2\_0\_data\_master\_read : in std\_logic := 'X'; -- read

nios2\_gen2\_0\_data\_master\_readdata : out std\_logic\_vector(31 downto 0); -- readdata

nios2\_gen2\_0\_data\_master\_write : in std\_logic := 'X'; -- write

nios2\_gen2\_0\_data\_master\_writedata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- writedata

nios2\_gen2\_0\_data\_master\_debugaccess : in std\_logic := 'X'; -- debugaccess

nios2\_gen2\_0\_instruction\_master\_address : in std\_logic\_vector(17 downto 0) := (others => 'X'); -- address

nios2\_gen2\_0\_instruction\_master\_waitrequest : out std\_logic; -- waitrequest

nios2\_gen2\_0\_instruction\_master\_read : in std\_logic := 'X'; -- read

nios2\_gen2\_0\_instruction\_master\_readdata : out std\_logic\_vector(31 downto 0); -- readdata

jtag\_uart\_0\_avalon\_jtag\_slave\_address : out std\_logic\_vector(0 downto 0); -- address

jtag\_uart\_0\_avalon\_jtag\_slave\_write : out std\_logic; -- write

jtag\_uart\_0\_avalon\_jtag\_slave\_read : out std\_logic; -- read

jtag\_uart\_0\_avalon\_jtag\_slave\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

jtag\_uart\_0\_avalon\_jtag\_slave\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

jtag\_uart\_0\_avalon\_jtag\_slave\_waitrequest : in std\_logic := 'X'; -- waitrequest

jtag\_uart\_0\_avalon\_jtag\_slave\_chipselect : out std\_logic; -- chipselect

nextval\_s1\_address : out std\_logic\_vector(1 downto 0); -- address

nextval\_s1\_write : out std\_logic; -- write

nextval\_s1\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

nextval\_s1\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

nextval\_s1\_chipselect : out std\_logic; -- chipselect

nextwriteval\_s1\_address : out std\_logic\_vector(1 downto 0); -- address

nextwriteval\_s1\_write : out std\_logic; -- write

nextwriteval\_s1\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

nextwriteval\_s1\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

nextwriteval\_s1\_chipselect : out std\_logic; -- chipselect

nios2\_gen2\_0\_debug\_mem\_slave\_address : out std\_logic\_vector(8 downto 0); -- address

nios2\_gen2\_0\_debug\_mem\_slave\_write : out std\_logic; -- write

nios2\_gen2\_0\_debug\_mem\_slave\_read : out std\_logic; -- read

nios2\_gen2\_0\_debug\_mem\_slave\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

nios2\_gen2\_0\_debug\_mem\_slave\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

nios2\_gen2\_0\_debug\_mem\_slave\_byteenable : out std\_logic\_vector(3 downto 0); -- byteenable

nios2\_gen2\_0\_debug\_mem\_slave\_waitrequest : in std\_logic := 'X'; -- waitrequest

nios2\_gen2\_0\_debug\_mem\_slave\_debugaccess : out std\_logic; -- debugaccess

onchip\_memory2\_0\_s1\_address : out std\_logic\_vector(13 downto 0); -- address

onchip\_memory2\_0\_s1\_write : out std\_logic; -- write

onchip\_memory2\_0\_s1\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

onchip\_memory2\_0\_s1\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

onchip\_memory2\_0\_s1\_byteenable : out std\_logic\_vector(3 downto 0); -- byteenable

onchip\_memory2\_0\_s1\_chipselect : out std\_logic; -- chipselect

onchip\_memory2\_0\_s1\_clken : out std\_logic; -- clken

readval\_s1\_address : out std\_logic\_vector(1 downto 0); -- address

readval\_s1\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

writeval\_s1\_address : out std\_logic\_vector(1 downto 0); -- address

writeval\_s1\_write : out std\_logic; -- write

writeval\_s1\_readdata : in std\_logic\_vector(31 downto 0) := (others => 'X'); -- readdata

writeval\_s1\_writedata : out std\_logic\_vector(31 downto 0); -- writedata

writeval\_s1\_chipselect : out std\_logic -- chipselect

);

end component MATRIX\_CALCULATOR\_mm\_interconnect\_0;

component MATRIX\_CALCULATOR\_irq\_mapper is

port (

clk : in std\_logic := 'X'; -- clk

reset : in std\_logic := 'X'; -- reset

receiver0\_irq : in std\_logic := 'X'; -- irq

sender\_irq : out std\_logic\_vector(31 downto 0) -- irq

);

end component MATRIX\_CALCULATOR\_irq\_mapper;

component altera\_reset\_controller is

generic (

NUM\_RESET\_INPUTS : integer := 6;

OUTPUT\_RESET\_SYNC\_EDGES : string := "deassert";

SYNC\_DEPTH : integer := 2;

RESET\_REQUEST\_PRESENT : integer := 0;

RESET\_REQ\_WAIT\_TIME : integer := 1;

MIN\_RST\_ASSERTION\_TIME : integer := 3;

RESET\_REQ\_EARLY\_DSRT\_TIME : integer := 1;

USE\_RESET\_REQUEST\_IN0 : integer := 0;

USE\_RESET\_REQUEST\_IN1 : integer := 0;

USE\_RESET\_REQUEST\_IN2 : integer := 0;

USE\_RESET\_REQUEST\_IN3 : integer := 0;

USE\_RESET\_REQUEST\_IN4 : integer := 0;

USE\_RESET\_REQUEST\_IN5 : integer := 0;

USE\_RESET\_REQUEST\_IN6 : integer := 0;

USE\_RESET\_REQUEST\_IN7 : integer := 0;

USE\_RESET\_REQUEST\_IN8 : integer := 0;

USE\_RESET\_REQUEST\_IN9 : integer := 0;

USE\_RESET\_REQUEST\_IN10 : integer := 0;

USE\_RESET\_REQUEST\_IN11 : integer := 0;

USE\_RESET\_REQUEST\_IN12 : integer := 0;

USE\_RESET\_REQUEST\_IN13 : integer := 0;

USE\_RESET\_REQUEST\_IN14 : integer := 0;

USE\_RESET\_REQUEST\_IN15 : integer := 0;

ADAPT\_RESET\_REQUEST : integer := 0

);

port (

reset\_in0 : in std\_logic := 'X'; -- reset

clk : in std\_logic := 'X'; -- clk

reset\_out : out std\_logic; -- reset

reset\_req : out std\_logic; -- reset\_req

reset\_req\_in0 : in std\_logic := 'X'; -- reset\_req

reset\_in1 : in std\_logic := 'X'; -- reset

reset\_req\_in1 : in std\_logic := 'X'; -- reset\_req

reset\_in2 : in std\_logic := 'X'; -- reset

reset\_req\_in2 : in std\_logic := 'X'; -- reset\_req

reset\_in3 : in std\_logic := 'X'; -- reset

reset\_req\_in3 : in std\_logic := 'X'; -- reset\_req

reset\_in4 : in std\_logic := 'X'; -- reset

reset\_req\_in4 : in std\_logic := 'X'; -- reset\_req

reset\_in5 : in std\_logic := 'X'; -- reset

reset\_req\_in5 : in std\_logic := 'X'; -- reset\_req

reset\_in6 : in std\_logic := 'X'; -- reset

reset\_req\_in6 : in std\_logic := 'X'; -- reset\_req

reset\_in7 : in std\_logic := 'X'; -- reset

reset\_req\_in7 : in std\_logic := 'X'; -- reset\_req

reset\_in8 : in std\_logic := 'X'; -- reset

reset\_req\_in8 : in std\_logic := 'X'; -- reset\_req

reset\_in9 : in std\_logic := 'X'; -- reset

reset\_req\_in9 : in std\_logic := 'X'; -- reset\_req

reset\_in10 : in std\_logic := 'X'; -- reset

reset\_req\_in10 : in std\_logic := 'X'; -- reset\_req

reset\_in11 : in std\_logic := 'X'; -- reset

reset\_req\_in11 : in std\_logic := 'X'; -- reset\_req

reset\_in12 : in std\_logic := 'X'; -- reset

reset\_req\_in12 : in std\_logic := 'X'; -- reset\_req

reset\_in13 : in std\_logic := 'X'; -- reset

reset\_req\_in13 : in std\_logic := 'X'; -- reset\_req

reset\_in14 : in std\_logic := 'X'; -- reset

reset\_req\_in14 : in std\_logic := 'X'; -- reset\_req

reset\_in15 : in std\_logic := 'X'; -- reset

reset\_req\_in15 : in std\_logic := 'X' -- reset\_req

);

end component altera\_reset\_controller;

signal nios2\_gen2\_0\_debug\_reset\_request\_reset : std\_logic; -- nios2\_gen2\_0:debug\_reset\_request -> rst\_controller:reset\_in0

signal nios2\_gen2\_0\_data\_master\_readdata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_readdata -> nios2\_gen2\_0:d\_readdata

signal nios2\_gen2\_0\_data\_master\_waitrequest : std\_logic; -- mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_waitrequest -> nios2\_gen2\_0:d\_waitrequest

signal nios2\_gen2\_0\_data\_master\_debugaccess : std\_logic; -- nios2\_gen2\_0:debug\_mem\_slave\_debugaccess\_to\_roms -> mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_debugaccess

signal nios2\_gen2\_0\_data\_master\_address : std\_logic\_vector(17 downto 0); -- nios2\_gen2\_0:d\_address -> mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_address

signal nios2\_gen2\_0\_data\_master\_byteenable : std\_logic\_vector(3 downto 0); -- nios2\_gen2\_0:d\_byteenable -> mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_byteenable

signal nios2\_gen2\_0\_data\_master\_read : std\_logic; -- nios2\_gen2\_0:d\_read -> mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_read

signal nios2\_gen2\_0\_data\_master\_write : std\_logic; -- nios2\_gen2\_0:d\_write -> mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_write

signal nios2\_gen2\_0\_data\_master\_writedata : std\_logic\_vector(31 downto 0); -- nios2\_gen2\_0:d\_writedata -> mm\_interconnect\_0:nios2\_gen2\_0\_data\_master\_writedata

signal nios2\_gen2\_0\_instruction\_master\_readdata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:nios2\_gen2\_0\_instruction\_master\_readdata -> nios2\_gen2\_0:i\_readdata

signal nios2\_gen2\_0\_instruction\_master\_waitrequest : std\_logic; -- mm\_interconnect\_0:nios2\_gen2\_0\_instruction\_master\_waitrequest -> nios2\_gen2\_0:i\_waitrequest

signal nios2\_gen2\_0\_instruction\_master\_address : std\_logic\_vector(17 downto 0); -- nios2\_gen2\_0:i\_address -> mm\_interconnect\_0:nios2\_gen2\_0\_instruction\_master\_address

signal nios2\_gen2\_0\_instruction\_master\_read : std\_logic; -- nios2\_gen2\_0:i\_read -> mm\_interconnect\_0:nios2\_gen2\_0\_instruction\_master\_read

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_chipselect : std\_logic; -- mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_chipselect -> jtag\_uart\_0:av\_chipselect

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_readdata : std\_logic\_vector(31 downto 0); -- jtag\_uart\_0:av\_readdata -> mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_readdata

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_waitrequest : std\_logic; -- jtag\_uart\_0:av\_waitrequest -> mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_waitrequest

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_address : std\_logic\_vector(0 downto 0); -- mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_address -> jtag\_uart\_0:av\_address

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read : std\_logic; -- mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_read -> mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read:in

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write : std\_logic; -- mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_write -> mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write:in

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_writedata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:jtag\_uart\_0\_avalon\_jtag\_slave\_writedata -> jtag\_uart\_0:av\_writedata

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_readdata : std\_logic\_vector(31 downto 0); -- nios2\_gen2\_0:debug\_mem\_slave\_readdata -> mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_readdata

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_waitrequest : std\_logic; -- nios2\_gen2\_0:debug\_mem\_slave\_waitrequest -> mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_waitrequest

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_debugaccess : std\_logic; -- mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_debugaccess -> nios2\_gen2\_0:debug\_mem\_slave\_debugaccess

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_address : std\_logic\_vector(8 downto 0); -- mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_address -> nios2\_gen2\_0:debug\_mem\_slave\_address

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_read : std\_logic; -- mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_read -> nios2\_gen2\_0:debug\_mem\_slave\_read

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_byteenable : std\_logic\_vector(3 downto 0); -- mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_byteenable -> nios2\_gen2\_0:debug\_mem\_slave\_byteenable

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_write : std\_logic; -- mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_write -> nios2\_gen2\_0:debug\_mem\_slave\_write

signal mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_writedata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:nios2\_gen2\_0\_debug\_mem\_slave\_writedata -> nios2\_gen2\_0:debug\_mem\_slave\_writedata

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_chipselect : std\_logic; -- mm\_interconnect\_0:onchip\_memory2\_0\_s1\_chipselect -> onchip\_memory2\_0:chipselect

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_readdata : std\_logic\_vector(31 downto 0); -- onchip\_memory2\_0:readdata -> mm\_interconnect\_0:onchip\_memory2\_0\_s1\_readdata

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_address : std\_logic\_vector(13 downto 0); -- mm\_interconnect\_0:onchip\_memory2\_0\_s1\_address -> onchip\_memory2\_0:address

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_byteenable : std\_logic\_vector(3 downto 0); -- mm\_interconnect\_0:onchip\_memory2\_0\_s1\_byteenable -> onchip\_memory2\_0:byteenable

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_write : std\_logic; -- mm\_interconnect\_0:onchip\_memory2\_0\_s1\_write -> onchip\_memory2\_0:write

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_writedata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:onchip\_memory2\_0\_s1\_writedata -> onchip\_memory2\_0:writedata

signal mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_clken : std\_logic; -- mm\_interconnect\_0:onchip\_memory2\_0\_s1\_clken -> onchip\_memory2\_0:clken

signal mm\_interconnect\_0\_readval\_s1\_readdata : std\_logic\_vector(31 downto 0); -- readval:readdata -> mm\_interconnect\_0:readval\_s1\_readdata

signal mm\_interconnect\_0\_readval\_s1\_address : std\_logic\_vector(1 downto 0); -- mm\_interconnect\_0:readval\_s1\_address -> readval:address

signal mm\_interconnect\_0\_nextval\_s1\_chipselect : std\_logic; -- mm\_interconnect\_0:nextval\_s1\_chipselect -> nextval:chipselect

signal mm\_interconnect\_0\_nextval\_s1\_readdata : std\_logic\_vector(31 downto 0); -- nextval:readdata -> mm\_interconnect\_0:nextval\_s1\_readdata

signal mm\_interconnect\_0\_nextval\_s1\_address : std\_logic\_vector(1 downto 0); -- mm\_interconnect\_0:nextval\_s1\_address -> nextval:address

signal mm\_interconnect\_0\_nextval\_s1\_write : std\_logic; -- mm\_interconnect\_0:nextval\_s1\_write -> mm\_interconnect\_0\_nextval\_s1\_write:in

signal mm\_interconnect\_0\_nextval\_s1\_writedata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:nextval\_s1\_writedata -> nextval:writedata

signal mm\_interconnect\_0\_writeval\_s1\_chipselect : std\_logic; -- mm\_interconnect\_0:writeval\_s1\_chipselect -> writeval:chipselect

signal mm\_interconnect\_0\_writeval\_s1\_readdata : std\_logic\_vector(31 downto 0); -- writeval:readdata -> mm\_interconnect\_0:writeval\_s1\_readdata

signal mm\_interconnect\_0\_writeval\_s1\_address : std\_logic\_vector(1 downto 0); -- mm\_interconnect\_0:writeval\_s1\_address -> writeval:address

signal mm\_interconnect\_0\_writeval\_s1\_write : std\_logic; -- mm\_interconnect\_0:writeval\_s1\_write -> mm\_interconnect\_0\_writeval\_s1\_write:in

signal mm\_interconnect\_0\_writeval\_s1\_writedata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:writeval\_s1\_writedata -> writeval:writedata

signal mm\_interconnect\_0\_nextwriteval\_s1\_chipselect : std\_logic; -- mm\_interconnect\_0:nextwriteval\_s1\_chipselect -> nextwriteval:chipselect

signal mm\_interconnect\_0\_nextwriteval\_s1\_readdata : std\_logic\_vector(31 downto 0); -- nextwriteval:readdata -> mm\_interconnect\_0:nextwriteval\_s1\_readdata

signal mm\_interconnect\_0\_nextwriteval\_s1\_address : std\_logic\_vector(1 downto 0); -- mm\_interconnect\_0:nextwriteval\_s1\_address -> nextwriteval:address

signal mm\_interconnect\_0\_nextwriteval\_s1\_write : std\_logic; -- mm\_interconnect\_0:nextwriteval\_s1\_write -> mm\_interconnect\_0\_nextwriteval\_s1\_write:in

signal mm\_interconnect\_0\_nextwriteval\_s1\_writedata : std\_logic\_vector(31 downto 0); -- mm\_interconnect\_0:nextwriteval\_s1\_writedata -> nextwriteval:writedata

signal irq\_mapper\_receiver0\_irq : std\_logic; -- jtag\_uart\_0:av\_irq -> irq\_mapper:receiver0\_irq

signal nios2\_gen2\_0\_irq\_irq : std\_logic\_vector(31 downto 0); -- irq\_mapper:sender\_irq -> nios2\_gen2\_0:irq

signal rst\_controller\_reset\_out\_reset : std\_logic; -- rst\_controller:reset\_out -> [irq\_mapper:reset, mm\_interconnect\_0:nios2\_gen2\_0\_reset\_reset\_bridge\_in\_reset\_reset, onchip\_memory2\_0:reset, rst\_controller\_reset\_out\_reset:in, rst\_translator:in\_reset]

signal rst\_controller\_reset\_out\_reset\_req : std\_logic; -- rst\_controller:reset\_req -> [nios2\_gen2\_0:reset\_req, onchip\_memory2\_0:reset\_req, rst\_translator:reset\_req\_in]

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read\_ports\_inv : std\_logic; -- mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read:inv -> jtag\_uart\_0:av\_read\_n

signal mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write\_ports\_inv : std\_logic; -- mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write:inv -> jtag\_uart\_0:av\_write\_n

signal mm\_interconnect\_0\_nextval\_s1\_write\_ports\_inv : std\_logic; -- mm\_interconnect\_0\_nextval\_s1\_write:inv -> nextval:write\_n

signal mm\_interconnect\_0\_writeval\_s1\_write\_ports\_inv : std\_logic; -- mm\_interconnect\_0\_writeval\_s1\_write:inv -> writeval:write\_n

signal mm\_interconnect\_0\_nextwriteval\_s1\_write\_ports\_inv : std\_logic; -- mm\_interconnect\_0\_nextwriteval\_s1\_write:inv -> nextwriteval:write\_n

signal rst\_controller\_reset\_out\_reset\_ports\_inv : std\_logic; -- rst\_controller\_reset\_out\_reset:inv -> [jtag\_uart\_0:rst\_n, nextval:reset\_n, nextwriteval:reset\_n, nios2\_gen2\_0:reset\_n, readval:reset\_n, writeval:reset\_n]

begin

jtag\_uart\_0 : component MATRIX\_CALCULATOR\_jtag\_uart\_0

port map (

clk => clk\_clk, -- clk.clk

rst\_n => rst\_controller\_reset\_out\_reset\_ports\_inv, -- reset.reset\_n

av\_chipselect => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_chipselect, -- avalon\_jtag\_slave.chipselect

av\_address => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_address(0), -- .address

av\_read\_n => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read\_ports\_inv, -- .read\_n

av\_readdata => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_readdata, -- .readdata

av\_write\_n => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write\_ports\_inv, -- .write\_n

av\_writedata => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_writedata, -- .writedata

av\_waitrequest => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_waitrequest, -- .waitrequest

av\_irq => irq\_mapper\_receiver0\_irq -- irq.irq

);

nextval : component MATRIX\_CALCULATOR\_nextval

port map (

clk => clk\_clk, -- clk.clk

reset\_n => rst\_controller\_reset\_out\_reset\_ports\_inv, -- reset.reset\_n

address => mm\_interconnect\_0\_nextval\_s1\_address, -- s1.address

write\_n => mm\_interconnect\_0\_nextval\_s1\_write\_ports\_inv, -- .write\_n

writedata => mm\_interconnect\_0\_nextval\_s1\_writedata, -- .writedata

chipselect => mm\_interconnect\_0\_nextval\_s1\_chipselect, -- .chipselect

readdata => mm\_interconnect\_0\_nextval\_s1\_readdata, -- .readdata

out\_port => nextval\_external\_connection\_export -- external\_connection.export

);

nextwriteval : component MATRIX\_CALCULATOR\_nextval

port map (

clk => clk\_clk, -- clk.clk

reset\_n => rst\_controller\_reset\_out\_reset\_ports\_inv, -- reset.reset\_n

address => mm\_interconnect\_0\_nextwriteval\_s1\_address, -- s1.address

write\_n => mm\_interconnect\_0\_nextwriteval\_s1\_write\_ports\_inv, -- .write\_n

writedata => mm\_interconnect\_0\_nextwriteval\_s1\_writedata, -- .writedata

chipselect => mm\_interconnect\_0\_nextwriteval\_s1\_chipselect, -- .chipselect

readdata => mm\_interconnect\_0\_nextwriteval\_s1\_readdata, -- .readdata

out\_port => nextwriteval\_external\_connection\_export -- external\_connection.export

);

nios2\_gen2\_0 : component MATRIX\_CALCULATOR\_nios2\_gen2\_0

port map (

clk => clk\_clk, -- clk.clk

reset\_n => rst\_controller\_reset\_out\_reset\_ports\_inv, -- reset.reset\_n

reset\_req => rst\_controller\_reset\_out\_reset\_req, -- .reset\_req

d\_address => nios2\_gen2\_0\_data\_master\_address, -- data\_master.address

d\_byteenable => nios2\_gen2\_0\_data\_master\_byteenable, -- .byteenable

d\_read => nios2\_gen2\_0\_data\_master\_read, -- .read

d\_readdata => nios2\_gen2\_0\_data\_master\_readdata, -- .readdata

d\_waitrequest => nios2\_gen2\_0\_data\_master\_waitrequest, -- .waitrequest

d\_write => nios2\_gen2\_0\_data\_master\_write, -- .write

d\_writedata => nios2\_gen2\_0\_data\_master\_writedata, -- .writedata

debug\_mem\_slave\_debugaccess\_to\_roms => nios2\_gen2\_0\_data\_master\_debugaccess, -- .debugaccess

i\_address => nios2\_gen2\_0\_instruction\_master\_address, -- instruction\_master.address

i\_read => nios2\_gen2\_0\_instruction\_master\_read, -- .read

i\_readdata => nios2\_gen2\_0\_instruction\_master\_readdata, -- .readdata

i\_waitrequest => nios2\_gen2\_0\_instruction\_master\_waitrequest, -- .waitrequest

irq => nios2\_gen2\_0\_irq\_irq, -- irq.irq

debug\_reset\_request => nios2\_gen2\_0\_debug\_reset\_request\_reset, -- debug\_reset\_request.reset

debug\_mem\_slave\_address => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_address, -- debug\_mem\_slave.address

debug\_mem\_slave\_byteenable => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_byteenable, -- .byteenable

debug\_mem\_slave\_debugaccess => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_debugaccess, -- .debugaccess

debug\_mem\_slave\_read => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_read, -- .read

debug\_mem\_slave\_readdata => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_readdata, -- .readdata

debug\_mem\_slave\_waitrequest => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_waitrequest, -- .waitrequest

debug\_mem\_slave\_write => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_write, -- .write

debug\_mem\_slave\_writedata => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_writedata, -- .writedata

dummy\_ci\_port => open -- custom\_instruction\_master.readra

);

onchip\_memory2\_0 : component MATRIX\_CALCULATOR\_onchip\_memory2\_0

port map (

clk => clk\_clk, -- clk1.clk

address => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_address, -- s1.address

clken => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_clken, -- .clken

chipselect => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_chipselect, -- .chipselect

write => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_write, -- .write

readdata => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_readdata, -- .readdata

writedata => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_writedata, -- .writedata

byteenable => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_byteenable, -- .byteenable

reset => rst\_controller\_reset\_out\_reset, -- reset1.reset

reset\_req => rst\_controller\_reset\_out\_reset\_req, -- .reset\_req

freeze => '0' -- (terminated)

);

readval : component MATRIX\_CALCULATOR\_readval

port map (

clk => clk\_clk, -- clk.clk

reset\_n => rst\_controller\_reset\_out\_reset\_ports\_inv, -- reset.reset\_n

address => mm\_interconnect\_0\_readval\_s1\_address, -- s1.address

readdata => mm\_interconnect\_0\_readval\_s1\_readdata, -- .readdata

in\_port => readval\_external\_connection\_export -- external\_connection.export

);

writeval : component MATRIX\_CALCULATOR\_nextval

port map (

clk => clk\_clk, -- clk.clk

reset\_n => rst\_controller\_reset\_out\_reset\_ports\_inv, -- reset.reset\_n

address => mm\_interconnect\_0\_writeval\_s1\_address, -- s1.address

write\_n => mm\_interconnect\_0\_writeval\_s1\_write\_ports\_inv, -- .write\_n

writedata => mm\_interconnect\_0\_writeval\_s1\_writedata, -- .writedata

chipselect => mm\_interconnect\_0\_writeval\_s1\_chipselect, -- .chipselect

readdata => mm\_interconnect\_0\_writeval\_s1\_readdata, -- .readdata

out\_port => writeval\_external\_connection\_export -- external\_connection.export

);

mm\_interconnect\_0 : component MATRIX\_CALCULATOR\_mm\_interconnect\_0

port map (

clk\_0\_clk\_clk => clk\_clk, -- clk\_0\_clk.clk

nios2\_gen2\_0\_reset\_reset\_bridge\_in\_reset\_reset => rst\_controller\_reset\_out\_reset, -- nios2\_gen2\_0\_reset\_reset\_bridge\_in\_reset.reset

nios2\_gen2\_0\_data\_master\_address => nios2\_gen2\_0\_data\_master\_address, -- nios2\_gen2\_0\_data\_master.address

nios2\_gen2\_0\_data\_master\_waitrequest => nios2\_gen2\_0\_data\_master\_waitrequest, -- .waitrequest

nios2\_gen2\_0\_data\_master\_byteenable => nios2\_gen2\_0\_data\_master\_byteenable, -- .byteenable

nios2\_gen2\_0\_data\_master\_read => nios2\_gen2\_0\_data\_master\_read, -- .read

nios2\_gen2\_0\_data\_master\_readdata => nios2\_gen2\_0\_data\_master\_readdata, -- .readdata

nios2\_gen2\_0\_data\_master\_write => nios2\_gen2\_0\_data\_master\_write, -- .write

nios2\_gen2\_0\_data\_master\_writedata => nios2\_gen2\_0\_data\_master\_writedata, -- .writedata

nios2\_gen2\_0\_data\_master\_debugaccess => nios2\_gen2\_0\_data\_master\_debugaccess, -- .debugaccess

nios2\_gen2\_0\_instruction\_master\_address => nios2\_gen2\_0\_instruction\_master\_address, -- nios2\_gen2\_0\_instruction\_master.address

nios2\_gen2\_0\_instruction\_master\_waitrequest => nios2\_gen2\_0\_instruction\_master\_waitrequest, -- .waitrequest

nios2\_gen2\_0\_instruction\_master\_read => nios2\_gen2\_0\_instruction\_master\_read, -- .read

nios2\_gen2\_0\_instruction\_master\_readdata => nios2\_gen2\_0\_instruction\_master\_readdata, -- .readdata

jtag\_uart\_0\_avalon\_jtag\_slave\_address => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_address, -- jtag\_uart\_0\_avalon\_jtag\_slave.address

jtag\_uart\_0\_avalon\_jtag\_slave\_write => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write, -- .write

jtag\_uart\_0\_avalon\_jtag\_slave\_read => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read, -- .read

jtag\_uart\_0\_avalon\_jtag\_slave\_readdata => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_readdata, -- .readdata

jtag\_uart\_0\_avalon\_jtag\_slave\_writedata => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_writedata, -- .writedata

jtag\_uart\_0\_avalon\_jtag\_slave\_waitrequest => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_waitrequest, -- .waitrequest

jtag\_uart\_0\_avalon\_jtag\_slave\_chipselect => mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_chipselect, -- .chipselect

nextval\_s1\_address => mm\_interconnect\_0\_nextval\_s1\_address, -- nextval\_s1.address

nextval\_s1\_write => mm\_interconnect\_0\_nextval\_s1\_write, -- .write

nextval\_s1\_readdata => mm\_interconnect\_0\_nextval\_s1\_readdata, -- .readdata

nextval\_s1\_writedata => mm\_interconnect\_0\_nextval\_s1\_writedata, -- .writedata

nextval\_s1\_chipselect => mm\_interconnect\_0\_nextval\_s1\_chipselect, -- .chipselect

nextwriteval\_s1\_address => mm\_interconnect\_0\_nextwriteval\_s1\_address, -- nextwriteval\_s1.address

nextwriteval\_s1\_write => mm\_interconnect\_0\_nextwriteval\_s1\_write, -- .write

nextwriteval\_s1\_readdata => mm\_interconnect\_0\_nextwriteval\_s1\_readdata, -- .readdata

nextwriteval\_s1\_writedata => mm\_interconnect\_0\_nextwriteval\_s1\_writedata, -- .writedata

nextwriteval\_s1\_chipselect => mm\_interconnect\_0\_nextwriteval\_s1\_chipselect, -- .chipselect

nios2\_gen2\_0\_debug\_mem\_slave\_address => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_address, -- nios2\_gen2\_0\_debug\_mem\_slave.address

nios2\_gen2\_0\_debug\_mem\_slave\_write => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_write, -- .write

nios2\_gen2\_0\_debug\_mem\_slave\_read => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_read, -- .read

nios2\_gen2\_0\_debug\_mem\_slave\_readdata => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_readdata, -- .readdata

nios2\_gen2\_0\_debug\_mem\_slave\_writedata => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_writedata, -- .writedata

nios2\_gen2\_0\_debug\_mem\_slave\_byteenable => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_byteenable, -- .byteenable

nios2\_gen2\_0\_debug\_mem\_slave\_waitrequest => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_waitrequest, -- .waitrequest

nios2\_gen2\_0\_debug\_mem\_slave\_debugaccess => mm\_interconnect\_0\_nios2\_gen2\_0\_debug\_mem\_slave\_debugaccess, -- .debugaccess

onchip\_memory2\_0\_s1\_address => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_address, -- onchip\_memory2\_0\_s1.address

onchip\_memory2\_0\_s1\_write => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_write, -- .write

onchip\_memory2\_0\_s1\_readdata => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_readdata, -- .readdata

onchip\_memory2\_0\_s1\_writedata => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_writedata, -- .writedata

onchip\_memory2\_0\_s1\_byteenable => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_byteenable, -- .byteenable

onchip\_memory2\_0\_s1\_chipselect => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_chipselect, -- .chipselect

onchip\_memory2\_0\_s1\_clken => mm\_interconnect\_0\_onchip\_memory2\_0\_s1\_clken, -- .clken

readval\_s1\_address => mm\_interconnect\_0\_readval\_s1\_address, -- readval\_s1.address

readval\_s1\_readdata => mm\_interconnect\_0\_readval\_s1\_readdata, -- .readdata

writeval\_s1\_address => mm\_interconnect\_0\_writeval\_s1\_address, -- writeval\_s1.address

writeval\_s1\_write => mm\_interconnect\_0\_writeval\_s1\_write, -- .write

writeval\_s1\_readdata => mm\_interconnect\_0\_writeval\_s1\_readdata, -- .readdata

writeval\_s1\_writedata => mm\_interconnect\_0\_writeval\_s1\_writedata, -- .writedata

writeval\_s1\_chipselect => mm\_interconnect\_0\_writeval\_s1\_chipselect -- .chipselect

);

irq\_mapper : component MATRIX\_CALCULATOR\_irq\_mapper

port map (

clk => clk\_clk, -- clk.clk

reset => rst\_controller\_reset\_out\_reset, -- clk\_reset.reset

receiver0\_irq => irq\_mapper\_receiver0\_irq, -- receiver0.irq

sender\_irq => nios2\_gen2\_0\_irq\_irq -- sender.irq

);

rst\_controller : component altera\_reset\_controller

generic map (

NUM\_RESET\_INPUTS => 1,

OUTPUT\_RESET\_SYNC\_EDGES => "deassert",

SYNC\_DEPTH => 2,

RESET\_REQUEST\_PRESENT => 1,

RESET\_REQ\_WAIT\_TIME => 1,

MIN\_RST\_ASSERTION\_TIME => 3,

RESET\_REQ\_EARLY\_DSRT\_TIME => 1,

USE\_RESET\_REQUEST\_IN0 => 0,

USE\_RESET\_REQUEST\_IN1 => 0,

USE\_RESET\_REQUEST\_IN2 => 0,

USE\_RESET\_REQUEST\_IN3 => 0,

USE\_RESET\_REQUEST\_IN4 => 0,

USE\_RESET\_REQUEST\_IN5 => 0,

USE\_RESET\_REQUEST\_IN6 => 0,

USE\_RESET\_REQUEST\_IN7 => 0,

USE\_RESET\_REQUEST\_IN8 => 0,

USE\_RESET\_REQUEST\_IN9 => 0,

USE\_RESET\_REQUEST\_IN10 => 0,

USE\_RESET\_REQUEST\_IN11 => 0,

USE\_RESET\_REQUEST\_IN12 => 0,

USE\_RESET\_REQUEST\_IN13 => 0,

USE\_RESET\_REQUEST\_IN14 => 0,

USE\_RESET\_REQUEST\_IN15 => 0,

ADAPT\_RESET\_REQUEST => 0

)

port map (

reset\_in0 => nios2\_gen2\_0\_debug\_reset\_request\_reset, -- reset\_in0.reset

clk => clk\_clk, -- clk.clk

reset\_out => rst\_controller\_reset\_out\_reset, -- reset\_out.reset

reset\_req => rst\_controller\_reset\_out\_reset\_req, -- .reset\_req

reset\_req\_in0 => '0', -- (terminated)

reset\_in1 => '0', -- (terminated)

reset\_req\_in1 => '0', -- (terminated)

reset\_in2 => '0', -- (terminated)

reset\_req\_in2 => '0', -- (terminated)

reset\_in3 => '0', -- (terminated)

reset\_req\_in3 => '0', -- (terminated)

reset\_in4 => '0', -- (terminated)

reset\_req\_in4 => '0', -- (terminated)

reset\_in5 => '0', -- (terminated)

reset\_req\_in5 => '0', -- (terminated)

reset\_in6 => '0', -- (terminated)

reset\_req\_in6 => '0', -- (terminated)

reset\_in7 => '0', -- (terminated)

reset\_req\_in7 => '0', -- (terminated)

reset\_in8 => '0', -- (terminated)

reset\_req\_in8 => '0', -- (terminated)

reset\_in9 => '0', -- (terminated)

reset\_req\_in9 => '0', -- (terminated)

reset\_in10 => '0', -- (terminated)

reset\_req\_in10 => '0', -- (terminated)

reset\_in11 => '0', -- (terminated)

reset\_req\_in11 => '0', -- (terminated)

reset\_in12 => '0', -- (terminated)

reset\_req\_in12 => '0', -- (terminated)

reset\_in13 => '0', -- (terminated)

reset\_req\_in13 => '0', -- (terminated)

reset\_in14 => '0', -- (terminated)

reset\_req\_in14 => '0', -- (terminated)

reset\_in15 => '0', -- (terminated)

reset\_req\_in15 => '0' -- (terminated)

);

mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read\_ports\_inv <= not mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_read;

mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write\_ports\_inv <= not mm\_interconnect\_0\_jtag\_uart\_0\_avalon\_jtag\_slave\_write;

mm\_interconnect\_0\_nextval\_s1\_write\_ports\_inv <= not mm\_interconnect\_0\_nextval\_s1\_write;

mm\_interconnect\_0\_writeval\_s1\_write\_ports\_inv <= not mm\_interconnect\_0\_writeval\_s1\_write;

mm\_interconnect\_0\_nextwriteval\_s1\_write\_ports\_inv <= not mm\_interconnect\_0\_nextwriteval\_s1\_write;

rst\_controller\_reset\_out\_reset\_ports\_inv <= not rst\_controller\_reset\_out\_reset;

end architecture rtl; -- of MATRIX\_CALCULATOR

**VHDL code for UART Decoder**

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

USE ieee.numeric\_std.all;

ENTITY Uart\_Decoder IS

GENERIC(

BaudRate : IN INTEGER := 9600;

ClockRate : IN INTEGER := 50\_000\_000

);

PORT(

Clk, Rx : IN STD\_LOGIC;

Complete : OUT STD\_LOGIC;

Data : OUT STD\_LOGIC\_VECTOR(7 DOWNTO 0)

);

END Uart\_Decoder;

ARCHITECTURE Behavior OF Uart\_Decoder IS

SIGNAL started : STD\_LOGIC; -- Whether we've started or not

SIGNAL bit\_location : Integer RANGE 0 TO 9 := 0; -- Where to save the bit

SIGNAL data\_reg : STD\_LOGIC\_VECTOR(9 DOWNTO 0); -- Local copy of the data, including start and stop bit

BEGIN

PROCESS (Rx, bit\_location)

BEGIN

IF bit\_location = 9 THEN

started <= '0';

ELSIF Rx = '0' AND Rx'event THEN

started <= '1';

END IF;

END PROCESS;

PROCESS (Clk, Rx, started)

VARIABLE counter : Integer RANGE 0 TO ((ClockRate / BaudRate)+1) := 0;

BEGIN

IF Clk = '1' AND Clk'event THEN

IF started = '1' THEN

counter := counter + 1;

IF counter = ((ClockRate) / BaudRate) THEN

counter := 0;

bit\_location <= bit\_location + 1;

ELSIF counter = (ClockRate / (BaudRate \* 2)) THEN

data\_reg(bit\_location) <= Rx;

END IF;

ELSE

bit\_location <= 0;

counter := 0;

END IF;

END IF;

END PROCESS;

Complete <= NOT started;

Data <= data\_reg(8 DOWNTO 1);

END Behavior;

**VHDL code for UART Transmitter:**

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

USE ieee.numeric\_std.all;

ENTITY Uart\_Transmitter IS

GENERIC(

BaudRate : IN INTEGER := 9600;

ClockRate : IN INTEGER := 50\_000\_000

);

PORT(

Clk, Send : IN STD\_LOGIC;

Data : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

Tx : OUT STD\_LOGIC

);

END Uart\_Transmitter;

ARCHITECTURE Behavior OF Uart\_Transmitter IS

SIGNAL started : STD\_LOGIC; -- Whether we've started or not

SIGNAL bit\_location : Integer RANGE 0 TO 9 := 0; -- Where to save the bit

BEGIN

PROCESS (Send, bit\_location)

BEGIN

IF bit\_location = 9 THEN

started <= '0';

ELSIF Send = '1' AND Send'event THEN

started <= '1';

END IF;

END PROCESS;

PROCESS (Clk, started, Data)

VARIABLE counter : Integer RANGE 0 TO ((ClockRate\*2) / BaudRate) := 0;

BEGIN

IF Clk = '1' AND Clk'event THEN

IF started = '1' THEN

counter := counter + 1;

IF counter = ((ClockRate) / BaudRate) THEN

counter := 0;

bit\_location <= bit\_location + 1;

ELSIF counter = (ClockRate / (BaudRate\*2)) THEN

-- Send the start bit

IF(bit\_location = 0) THEN

Tx <= '0';

-- Send data bits

ELSIF bit\_location > 0 AND bit\_location < 9 THEN

Tx <= Data(bit\_location - 1);

-- Send the stop bit

ELSE

Tx <= '1';

END IF;

END IF;

ELSE

bit\_location <= 0;

counter := 0;

Tx <= '1';

END IF;

END IF;

END PROCESS;

END Behavior;

**VHDL code for FIFO:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity FIFO is

generic (num : in integer := 128);

port ( complete : in std\_logic;

data\_in : in std\_logic\_vector(7 downto 0);

pop, clear : in std\_logic;

data\_out : out std\_logic\_vector (7 downto 0));

end FIFO;

architecture behavior of FIFO is

type fifo\_size is array (0 to num-1) of std\_logic\_vector (7 downto 0);

signal mem : fifo\_size; --declaring 32 buffers with 8 bit wide

signal stop : integer range 0 to num-1 := 0;

signal start : integer range 0 to num-1 := 0;

begin

--at the rising edge of complete

--data is received into buffer

--if index of mem reaches num (32) the index is changed ot 0

process(complete, pop, data\_in, clear)

variable newStart : integer range 0 to num-1;

variable newEnd : integer range 0 to num-1;

variable toSend : std\_logic\_vector(7 downto 0);

begin

if clear = '1' then

start <= 0;

stop <= 0;

else

if complete'event and complete = '1' then

newEnd := stop - 2;

if not(start = newEnd) then

start <= start + 1;

if(start = num-1) then

mem(0) <= data\_in;

else

mem(start + 1) <= data\_in;

end if;

end if;

end if;

--assuming pop as a 1 bit input

--first value from the queue is stored into data\_out object

--queue is updated

newStart := start;

if pop'event and pop = '1' then

if not (newStart = stop) then

stop <= stop + 1;

end if;

end if;

end if;

-- Get the current head of the ring buffer if we're not empty

if not (start = stop) then

if(stop = num - 1) then

toSend := mem(0);

else

toSend := mem(stop + 1);

end if;

else

toSend := "00000000";

end if;

data\_out <= toSend;

end process;

end;

**Nios C code:**

//declaration of header files

#include "sys/alt\_stdio.h"

#include "stdlib.h"

#include "stdio.h"

#include "math.h"

#include "stdint.h"

#include "io.h"

#include "altera\_avalon\_pio\_regs.h"

#include "string.h"

/\*\*

\*\*@brief – sends an indicator to UART Tx that next value is ready to be displayed on the terminal

\*/

void next\_write()

{

uint8\_t \*next;

next = (uint8\_t \*)0x00021000;

\*next = 0;

for(volatile uint32\_t i=0; i<500000;i++);

\*next = 1;

for(volatile uint32\_t i=0; i<500000;i++);

}

/\*\*

\*\*@brief – writeByte and writeString functions fetch the value to be displayed into a Parallel IO with address 0x00021010

\*the value from the parallel IO is sent to UART Tx to display on the remote terminal

\*/

void writeByte(char c)

{

char \*toSend;

toSend = (char \*)0x00021010;

\*toSend = c;

}

void writeString(char\* str, int len)

{

for(int i = 0; i < len; ++i) {

writeByte(str[i]);

next\_write();

}

}

/\*\*

\*\*@brief – sends an indicator to FIFO that next value is ready to be stored into a parallel IO

\*/

void next\_from\_pio()

{

uint8\_t \*next;

next = (uint8\_t \*)0x00021020;

\*next = 0;

for(volatile uint32\_t i=0; i<500000;i++);

\*next = 1;

for(volatile uint32\_t i=0; i<500000;i++);

}

/\*\*

\*\*@brief – decodes the ascii value present in the Parallel IO( with address -0x00021030) into a number

\*calls next\_from\_pio() function inorder to store new value from FIFO into Parallel IO

\*‘,’ (comma) is used as a delimiter while reading data from FIFO

\*/

int decode\_ascii() {

int retval = 0;

while(1) {

char value = IORD\_ALTERA\_AVALON\_PIO\_DATA(0x00021030);

printf("%c\n", value);

if(value == ',') break;

if(value >= '0' && value <= '9')

{

retval \*= 10;

retval += value-'0';

}

next\_from\_pio();

}

next\_from\_pio();

return retval;

}

/\*

/\*\*

\* @brief Adds to matrices together

\*

\* @param a First matrix to add

\* @param b Second matrix to add

\* @param r1 Number of rows in a

\* @param c1 Number of columns in a

\* @param r2 Number of rows in b

\* @param c2 Number of columns in b

\*/

void matrix\_add(int\*\* a, int\*\* b, int r1, int c1, int r2, int c2)

{

int i,j,k,l;

int res[r1][c1];

if (r1 != r2 || c2 != c1)

{

char s[100];

char disp[]="Cannot be added";

sprintf(s,"%s",disp);

writeString(s, strlen(s));

}

else

{

for (i=0;i<r1;i++)

{

for(j=0;j<c1;j++)

{

res[i][j]= a[i][j] + b[i][j];

}

}

}

for (i=0;i<r1;i++)

{

for(j=0;j<c1;j++)

{

printf("res[%d][%d]= %d\n",i,j,res[i][j]);

char s[100];

sprintf(s,"%d,",res[i][j]);

writeString(s, strlen(s));

}

}

}

/\*\*

\* @brief performs matrix subtraction

\*

\* @param a First matrix

\* @param b Second matrix

\* @param r1 Number of rows in a

\* @param c1 Number of columns in a

\* @param r2 Number of rows in b

\* @param c2 Number of columns in b

\*/

void matrix\_sub(int\*\* a, int\*\* b, int r1, int c1, int r2, int c2)

{

int i,j,k,l;

int res[r1][c1];

if (r1 != r2 || c2 != c1)

{

char s[100];

char disp[]="Cannot be subtracted";

sprintf(s,"%s",disp);

writeString(s, sizeof(s));

}

else

{

for (i=0;i<r1;i++)

{

for(j=0;j<c1;j++)

{

res[i][j]= a[i][j] - b[i][j];

}

}

}

for (i=0;i<r1;i++)

{

for(j=0;j<c1;j++)

{

printf("res[%d][%d]= %d\n",i,j,res[i][j]);

char s[100];

sprintf(s,"%d,",res[i][j]);

writeString(s, strlen(s));

}}}

/\*\*

\* @brief Multiplies two matrices together

\*

\* @param a First matrix

\* @param b Second matrix

\* @param r1 Number of rows in a

\* @param c1 Number of columns in a

\* @param r2 Number of rows in b

\* @param c2 Number of columns in b

\*/

void matrix\_mul(int\*\* a, int\*\* b, int r1, int c1, int r2, int c2)

{

int i,j,k,l,m;

int res[r1][c2];

if(c1 != r2)

{

char s[100];

char disp[]="Cannot be multiplied";

sprintf(s,"%s",disp);

writeString(s, sizeof(s));

}

else

{

for (i=0;i<r1;i++)

{

for(j=0;j<c2;j++)

{

res[i][j]=0;

for(m=0;m<c1;m++)

{

res[i][j]=res[i][j]+ (a[i][m] \* b[m][j]);

}

}

}

}

for (i=0;i<r1;i++)

{

for(j=0;j<c2;j++)

{

printf("res[%d][%d]= %d",i,j,res[i][j]);

char s[100];

sprintf(s,"%d,",res[i][j]);

writeString(s, strlen(s));

}}}

/\*scalar multiplication\*/

void scalar\_matrix\_mul (int \*\*a, int r1, int c1)

{

int i,j;

int k;

int res[r1][c1];

for (i=0; i<r1; i++)

{

for (j=0;j<c1;j++)

{

res[i][j]=k\*a[i][j];

}

}

for (i=0;i<r1;i++)

{

for(j=0;j<c1;j++)

{

printf("res[%d][%d]= %d\n",i,j,res[i][j]);

char s[100];

sprintf(s,"%d,",res[i][j]);

writeString(s, strlen(s));

}}}

/\*\*

\* @brief Calculates determinant of a matrix

\*

\* @param a First matrix whose determinant is calculated

\* @param r1 Number of rows in a

\* @param c1 Number of columns in a

\*/

int matrix\_det(int\*\* a, int r1, int c1)

{

int D ;

int D1;

int n;

int \*\*temp;

int i,j=0;

int sign = 1;

// Base case : if matrix contains single element

if(r1!=c1)

{

//not possible to find determinant

char s[100];

char disp[]="Cannot find determinant";

sprintf(s,"%s",disp);

writeString(s, strlen(s));

}

else

{

n=r1;

if (n == 1)

{

D=a[0][0];

return(D);

}

else

{

D=0;

// Iterate for each element of first row

for (int f = 0; f < n; f++)

{

// Getting Cofactor of a[0][f]

temp= malloc(2\*sizeof\*temp);

for (i=0; i< n; i++)

{

temp[i]= malloc(2\*sizeof\*temp[i]);

}

i=0;

// Looping for each element of the matrix

for (int row = 0; row < n; row++)

{

for (int col = 0; col < n; col++)

{

// Copying into temporary matrix only those

// element which are not in given row and

// column

if (row != 0 && col != f)

{

temp[i][j++] = a[row][col];

// Row is filled, so increase row index and

// reset col index

if (j == n - 1)

{

j = 0;

i++;

}

}

}

}

if(f%2==0)

{

( D += a[0][f]

\*(matrix\_det(temp, n - 1,n - 1)));

}

else

{

D -= a[0][f]

\*(matrix\_det(temp, n - 1,n - 1));

}

// terms are to be added with alternate sign

D1=D;

}

}

}

return D1;}

/\*\*

\* @brief Calculates transpose of a matrix

\*

\* @param a is the matrix whose transpose is calculated

\* @param r1 Number of rows in a

\* @param c1 Number of columns in a

\*/

void matrix\_transpose(int \*\*a, int r1, int c1)

{

int i,j;

int res[r1][c1];

for (i=0; i<c1;i++)

{

for (j=0;j<r1;j++)

{

res[i][j]= a[j][i];

}

}

for (i=0;i<c1;i++)

{

for(j=0;j<r1;j++)

{

printf("res[%d][%d]= %d\n",i,j,res[i][j]);

char s[100];

sprintf(s,"%d,",res[i][j]);

writeString(s, strlen(s));

}}}

/\*......Main Program ........\*/

int main()

{

int ROW1, ROW2, COL1, COL2;

int \*\*A;

int \*\*B ;

int Determinant\_A,Determinant\_B;

int OP\_SEL;

char str[100];

int i,j,k;

printf("entered main\n");

//reading row and column size for matrix A and B

// Read the row, column size of matrix 1 and matrix 2 from the FPGA PIO layer.

ROW1= decode\_ascii();

COL1=decode\_ascii();

ROW2=decode\_ascii();

COL2=decode\_ascii();

//reading values into matrix A and B

//allocating memory

A= malloc(ROW1\*sizeof\*A);

for (i=0; i< ROW1; i++)

{

A[i]= malloc(COL1\*sizeof\*A[i]);

}

B= malloc(ROW2\*sizeof\*B);

for (i=0; i< ROW2; i++)

{

B[i]= malloc(COL2\*sizeof\*B[i]);

}

for (i=0;i<ROW1; i++)

{

for(j=0;j<COL1;j++)

{

A[i][j]=decode\_ascii();

}

}

for (i=0;i<ROW2; i++)

{

for(j=0;j<COL2;j++)

{

B[i][j]=decode\_ascii();

} }

printf("ROW1=%d\n",ROW1);

printf("COL1=%d\n",COL1);

printf("ROW2=%d\n",ROW2);

printf("COL2=%d\n",COL2);

//reading valaue that indicates type of operation

OP\_SEL=decode\_ascii();

printf("%d\n",OP\_SEL);

switch (OP\_SEL){

case 1:

writeString("Addition selected\r\n",strlen("Addition selected\r\n"));

matrix\_add(A,B,ROW1,COL1, ROW2,COL2);

break;

case 2:

writeString("Subtraction selected\r\n",strlen("Subtraction selected\r\n"));

matrix\_sub(A,B,ROW1,COL1, ROW2,COL2);

break;

case 3:

writeString("Multiplication selected\r\n",strlen("Multiplication selected\r\n"));

matrix\_mul(A,B,ROW1,COL1, ROW2,COL2);

break;

case 4:

writeString("Determinant selected\r\n",strlen("Determinant selected\r\n"));

Determinant\_A=matrix\_det(A,ROW1,COL1);

sprintf(str,"%d\r\n",Determinant\_A);

writeString(str, strlen(str));

Determinant\_B=matrix\_det(B,ROW2,COL2);

sprintf(str,"%d",Determinant\_B);

writeString(str, strlen(str));

break;

case 5:

matrix\_transpose(A,ROW1,COL1);

break;

default:

writeString(“default selected”, strlen(“default selected”));

break;

}

//deallocating memory

free(A);

free(B);

return 0;

}

*End of document*